May 1990

─────────────────── PRODUCT PROFILE ───────────────────

FUJITSU

MB85411-*30/40*
CMOS STATIC RAM MODULE

65536 Words x 9-Bit

The Fujitsu MB85411 is a fully decoded, CMOS static random access memory module (SRAM) with nine MB81C71A devices mounted on a 70-pin Epoxy module. A separate SELECT pin provides parity capability. Additionally, these modules incorporate a presence detect feature that permits system level verification of memory density for those applications with multiple modules. Organized as nine 64K x 1 devices, the MB85411 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.
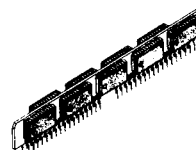
PRELIMINARY

PLASTIC PACKAGE
MZP–70P–P01

PIN ASSIGNMENT

- Organized as 65536 x 9-Bit Words
- Access Time/Cycle Time
  –30: 30 ns Max.
  –40: 40 ns Max.
- Low Power Dissipation
  Active: 3960 mW (Max)
  Standby: 495 mW
       CMOS Level
       990 mW
       TTL Level

- Static Operation
- Single +5 V ±10% Power Supply
- Parity Capability (D4, Q4)
- Separate Data Inputs and Outputs
- Input/Output Pins TTL Compatible
- 70-pin Epoxy Module (ZIP)
- Presence Detect: PD0 = GND;
           PD1 = Open
- Temperature Range: 0°C to 70°C

Pin			Pin
PD0	2	1	GND
DO	4	3	PD1
VCC	6	5	Q0
NC	8	7	NC
D1	10	9	NC
NC	12	11	Q1
NC	14	13	NC
D2	16	15	NC
GND	18	17	Q2
A1	20	19	A0
D3	22	21	A2
A3	24	23	Q3
A5	26	25	A4
D4	28	27	VCC
NC	30	29	Q4
W1	32	31	W2
NC	34	33	NC
		35	CS1
CS2	36	37	NC
NC	38	39	NC
A6	40	41	A7
D5	42	43	Q5
VCC	44	45	NC
A8	46	47	A9
A10	48	49	A11
D6	50	51	Q6
NC	52	53	GND
A12	54	55	A13
A14	56	57	A15
D7	58	59	Q7
NC	60	61	NC
NC	62	63	NC
NC	64	65	VCC
D8	66	67	Q8
NC	68	69	NC
GND	70		

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ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
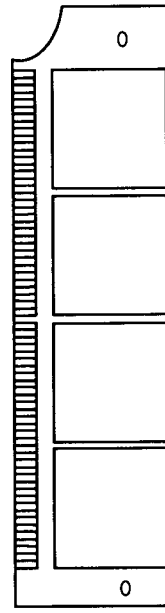
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address and $\overline{WE}$	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		40	pF
Input Capacitance, D_{IN}	C_{IN3}		10	pF
Output Capacitance, D_{OUT}	C_{OUT}		10	pF

DC CHARACTERISTICS
(At recommended operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VALUE			UNIT
			Min	Typ	Max	
Input Leakage Current (V_{IN} = OV to V_{CC})		I_{LI}	−80		80	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = OV to V_{CC})		I_{LO}	−10		10	μA
Standby Power Supply Current	CMOS level	I_{SB1}			90	mA
	TTL level	I_{SB2}			180	mA
Active Power Supply Current ($\overline{CS}$ = V_{IL}, I_{OUT} = O mA)		I_{CC}			720	mA
Peak Powe onr Supply Current ($\overline{CS}$ = Lower of V_{CC} pr V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level[1]		V_{IL}	−0.5		0.8	V
Output High Level (I_{OH} = −4 mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16 mA)		V_{OL}			0.4	V

Note: [1] −2.OV level with a maximum pulse width of 20 ns.

AC CHARACTERISTICS
(At recommended operating conditions unless otherwise noted)*

READ CYCLE

PARAMETER	SYM	MB85411–30 Min	MB85411–30 Max	MB85411–40 Min	MB85411–40 Max	UNIT	NOTE
Read Cycle Time	t_{RC}	30		40		ns	1
Address Access Time	t_{AA}		30		40	ns	
$\overline{CS}$ Access Time	t_{ACS}		30		40	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
$\overline{CS}$ to Output Low–Z	t_{LZ}	5		5		ns	3,4
$\overline{CS}$ to Output High–Z	t_{HZ}	0	10	0	15	ns	3,4
Power Up from $\overline{CS}$	t_{PU}	0		0		ns	
Power Down from $\overline{CS}$	t_{PD}		20		30	ns	

WRITE CYCLE

PARAMETER	SYM	MB85411–30 Min	MB85411–30 Max	MB85411–40 Min	MB85411–40 Max	UNIT	NOTE
Write Cycle Time	t_{WC}	30		40		ns	2
Address Valid to End of Write	t_{AW}	25		35		ns	
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns	
Data Hold Time	t_{DH}	2		2		ns	
Write Pulse Width	t_{WP}	20		30		ns	
Data Valid to End of Write	t_{DW}	15		20		ns	
Address Setup Time	t_{AS1}	0		0		ns	
Address Setup Time	t_{AS2}	0		0		ns	
Write Recovery Time	t_{WR}	2		2		ns	
Output to High–Z from $\overline{WE}$	t_{WZ}	0	10	0	15	ns	3,4
Output to Low–Z from $\overline{WE}$	t_{OW}	0		0		ns	3,4

Notes: * Refer to MB81C71A data sheet electricals for an explanation of the notes.
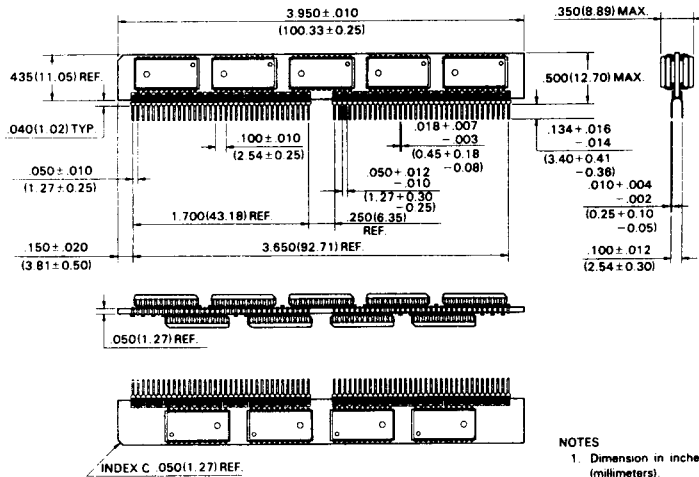
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MB85411-30/-40

FUNCTIONAL BLOCK DIAGRAM
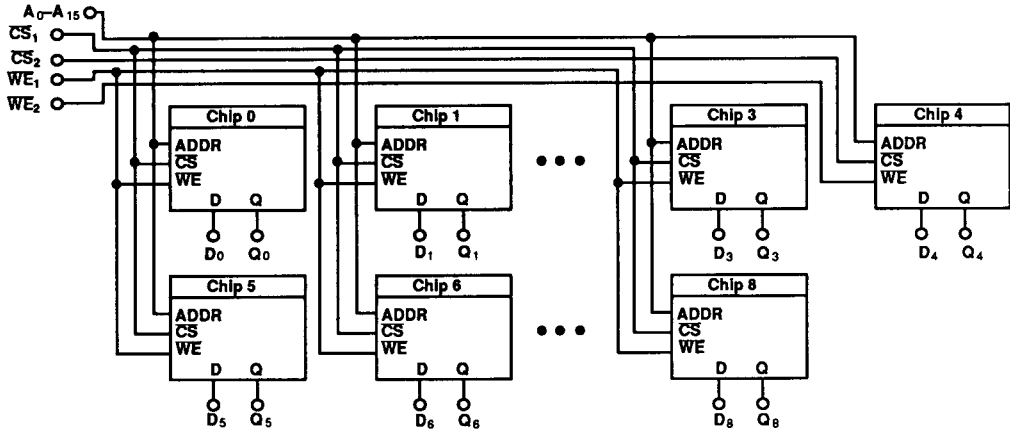
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PACKAGE DIMENSIONS

60-Lead Epoxy Module
(Case No.: MZP-70P-PO1)

NOTES
1. Dimension in inches and (millimeters).
2. Pin No. 1; Back side